# DAC8831/32 Evaluation Module

This user's guide describes the DAC8831/32 Evaluation Module. It covers the operating procedures and characteristics of the EVM board along with the device that it supports. The physical PCB layout, schematic diagram, and circuit descriptions are included.

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## 1 EVM Overview

This chapter provides an overview of the DAC8831/32 evaluation module (EVM), and instructions on setting up and using this evaluation module.

### *1.1 Features*

This EVM features the DAC8831/32 16-bit resolution, unbuffered voltage output digital-to-analog converter (DAC). This EVM supports the 14-pin QFN package (RGY) only for the DAC8831 and the DAC8832. The design is based on the modular EVM format for Data Acquisitions Product group of Texas Instruments to provide quick and easy way to evaluate the functionality and performance of the high-resolution serial input DAC. This EVM includes an onboard reference and buffer circuits and allows high speed serial interface with a variety of TI DSP and microcontroller interface boards.

## 1.2 Power Requirements

The following sections describe the power requirements of this EVM.

### 1.2.1 Supply Voltage

The DC power supply for the digital section ($V_{DD}$) of this EVM is dedicated to +5V via the J3-10 terminal and is referenced to ground through the J3-5 terminal.

The DC power supply requirements for the analog section of this EVM are as follows: the +5VA connects through J3-3 and the –5VA connects through J3-4. All the analog power supplies are referenced to analog ground through J3-6 terminal.

The device under test (U3) power supply only requires +5V to operate; therefore, the supply is derived from $V_{DD}$ (via J3-10). The +5VA supply sources the positive rail of the external output op-amp, U1, while –V, which is configurable between –5VA and AGND via R2 and R7 shorting resistors, supplies the negative rail of the output op-amp. The supply for the voltage reference circuit U5, as well as the reference buffer U4, uses +5VA, and their respective grounds are tied together in a star connection. The J3 header provides connection to the common power bus described in 5-6K Interface Board User's Guide (SLAU104). Table 1 shows the pinout of connector J3.

**Table 1. Pinout of J3**

| Signal | Pin Number | | Signal |
|---|---|---|---|
| Unused | 1 | 2 | Unused |
| +5VA | 3 | 4 | –5VA |
| DGND | 5 | 6 | AGND |
| Unused | 7 | 8 | Unused |
| Unused | 9 | 10 | +5VD |

**CAUTION**

To avoid potential damage to the EVM board, make sure that the correct cables are connected to their respective terminals as labeled on the EVM board.

Stresses above the maximum listed voltage ratings may cause permanent damage to the device.

### 1.2.2 Reference Voltage

The externally generated +2.5VDC precision voltage reference is jumper selectable via W1. The reference voltage can be selected either by the +2.5V onboard reference/buffer circuits (U4 and U5) or an external reference applied to J1-20. The EVM ships out of factory with the default position (shunt on W1 pins 1-2) of +2.5V reference that is supplied by REF3025 (U5), which is a 50ppm/°C with excellent line regulation and stability. The +2.5VDC reference will provide the DAC8831/32's voltage output range.

Moving the shunt at W1 to pins 2-3 allows an external reference applied to J1-20 to be used. Regardless of the reference source, U4 provides a reference buffer to the DAC8831/32. If no buffer circuit is desired, the EVM user can remove the resistor found at location R5 and apply an external reference directly to TP1, referenced to AGND.

## 1.3 EVM Basic Functions

This EVM is designed primarily as an evaluation platform to test certain functional characteristics of the DAC8831/32 digital-to-analog converter. The evaluation of the installed DAC device can be accomplished with the use of any microprocessor, TI DSP or an appropriate signal/waveform generator.

The headers J2 (top side) and P2 (bottom side) are pass through connectors provided to allow the control signals and data required to interface a host processor or waveform generator to the DAC8831/32 EVM using a custom built cable.

An adapter interface card (5-6k adapter interface) is also available to fit and mate with TI's TMS320C5000™ and C6000™ DSP Starter Kit (DSK). This alleviates the trouble involved in building a custom cable. In addition, there is also an MSP430-based platform (HPA449) that uses the MSP430F449 microprocessor, which this EVM can connect to and interface with as well. For more details or information regarding the 5-6k adapter interface card or the HPA449 platform, call Texas Instruments Incorporated or email us at dataconvapps@list.ti.com.

The buffered DAC output can be monitored through pin 2 of J1 header connector. The EVM also provides a provision for Kelvin sense connection to increase performance of the DAC. This option does not come factory installed, and the EVM user must provide the necessary parts and labor.

A block diagram of the DAC8831/32 EVM is shown in Figure 1 .

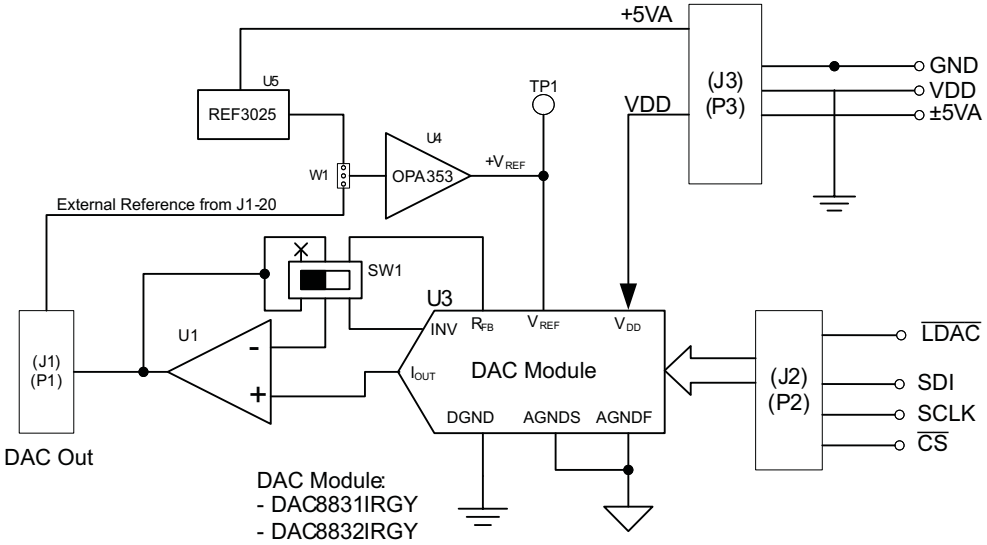



**Figure 1. DAC8831/32 EVM Block Diagram**

## 1.4 Related Documentation from Texas Instruments

To obtain a copy of any of the following TI documents, call the Texas Instruments Literature Response Center at (800) 477–8924 or the Product Information Center (PIC) at (972) 644–5580. When ordering, identify this manual by its title and literature number. Updated documents can also be obtained through our website at www.ti.com.

| DATA SHEETS: | LITERATURE NUMBER: |
|---|---|
| DAC8831 | SLAS449 |
| DAC8832 | SBAS380 |
| OPA735 | SBOS282 |
| OPA353 | SBOS103 |
| REF3025 | SBVS032 |

## 1.5 Questions about this or other Data Converter EVMs?

If you have questions about this or other Texas Instruments Data Converter evaluation modules, feel free to e-mail the Data Converter Application Team at dataconvapps@list.ti.com. Include in the subject heading the product you have questions or concerns with.

# 2 PCB Design and Performance

This section talks about the layout design of the PCB describing the physical and mechanical characteristics of the EVM. It shows the resulting performance of the EVM, which can be compared to the device specification listed in the datasheet. The list of components used on the module is also included in this section.

## 2.1 PCB Layout

The DAC8831/32 EVM is designed to demonstrate the performance quality of the installed DAC device under test, as specified in the datasheet. Careful analysis of the EVM's physical restrictions and factors that contributes to the EVM's performance degradation is the key to a successful design implementation. The obvious attributes that contributes to the poor performance of the EVM can be avoided during the schematic design phase by properly selecting the right components and designing the circuit correctly. The circuit should include adequate bypassing, identifying and managing the analog and digital signals and knowing or understanding the components mechanical attributes.

The obscure part of the design lies particularly in the layout process. The main concern is primarily with the placement of components and the proper routing of signals. The bypass capacitors should be placed as close as possible to the pins and the analog and digital signals should be properly separated from each other. The power and ground plane is very important and should be carefully considered in the layout process. A solid plane is ideally preferred but sometimes impractical, so when solid planes are not possible, a split plane will do the job as well. When considering a split plane design, analyze the component placement and carefully split the board into its analog and digital sections starting from the device under test. The ground plane plays an important role in controlling the noise and other effects that otherwise contributes to the error of the DAC output. To ensure that the return currents are handled properly, route the appropriate signals only in their respective sections; meaning, the analog traces should only be placed in the analog section, and the digital traces in the digital section. Minimize the length of the traces but use the biggest possible trace width allowable in the design. These design practice discussed can be seen in the following figures presented below.

The DAC8831/32 EVM board is constructed on a two-layer printed circuit board using a copper-clad FR-4 laminate material. The printed circuit board has a dimension of 43,1800 mm (1.7000 inch) × 82,5500 mm (3.2000 inch), and the board thickness is 1,5748 mm (0.0620 inch). Figure 2 through Figure 7 show the individual artwork layers.

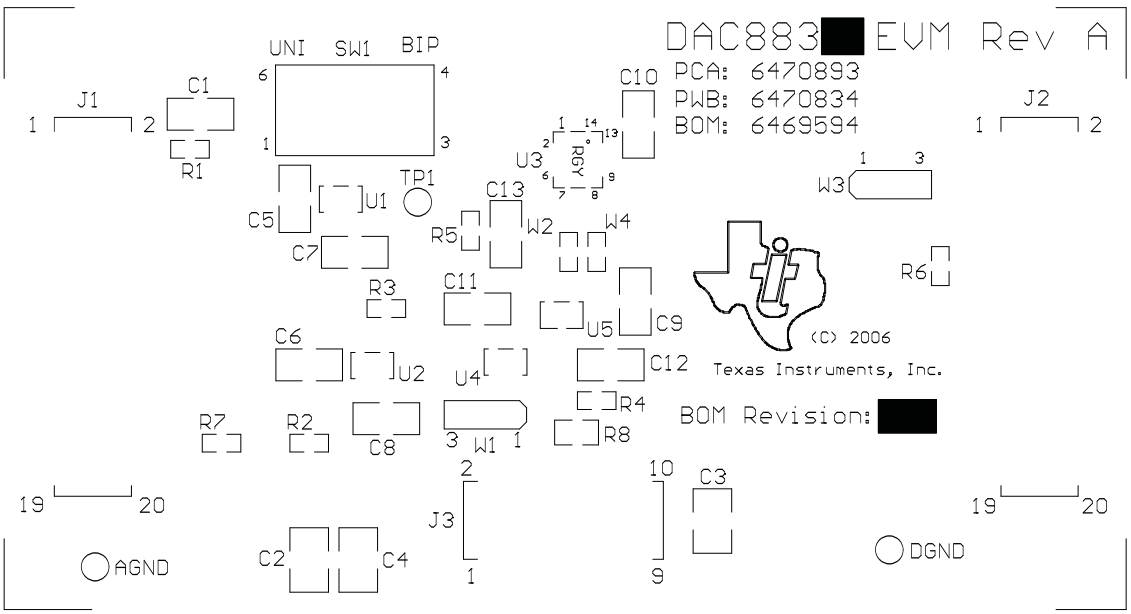



**Figure 2. Top Silkscreen**

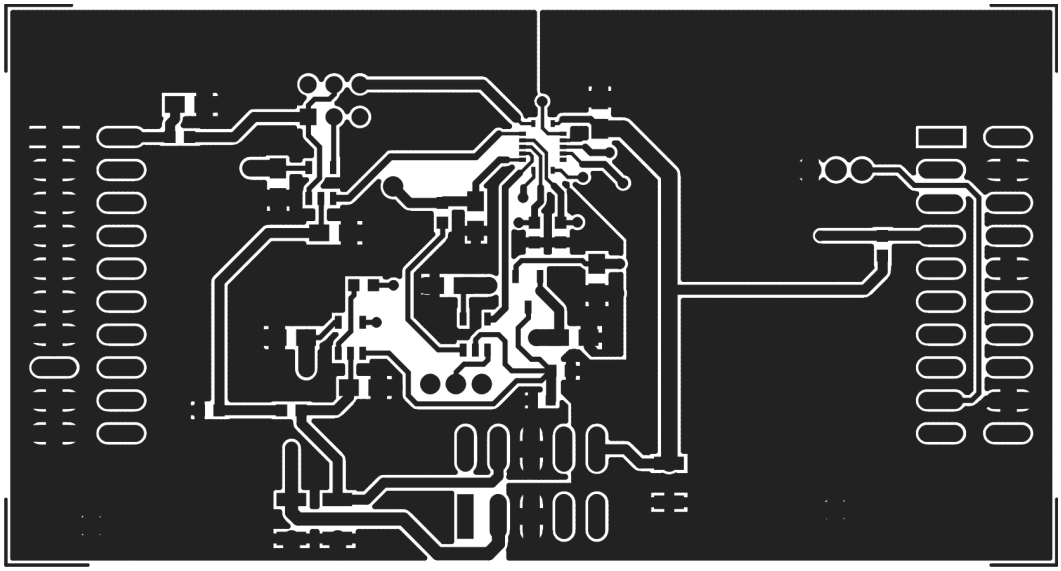


**Figure 3. Layer 1 (Top Layer)**

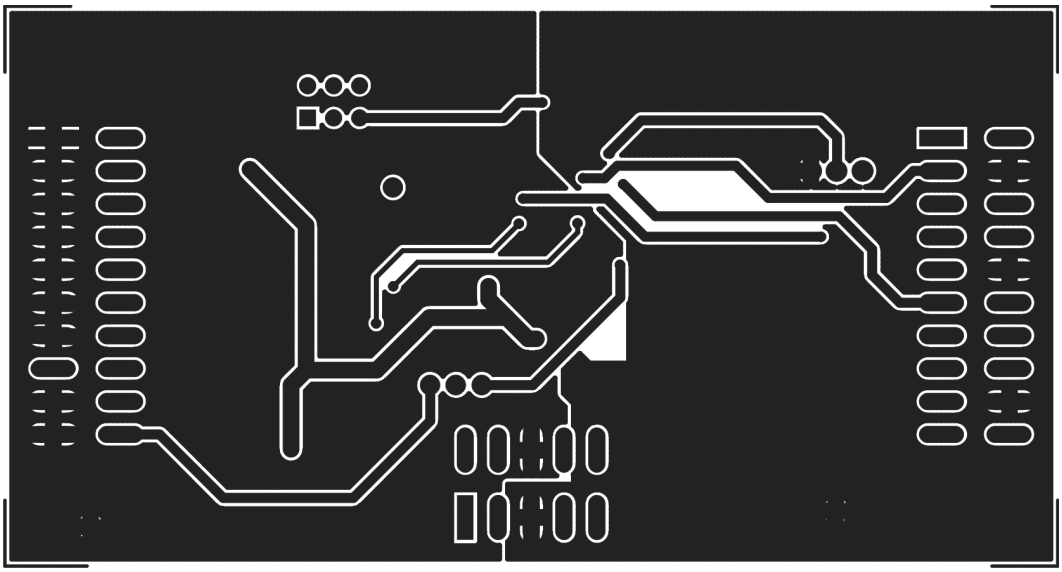


**Figure 4. Layer 2 (Bottom Layer)**

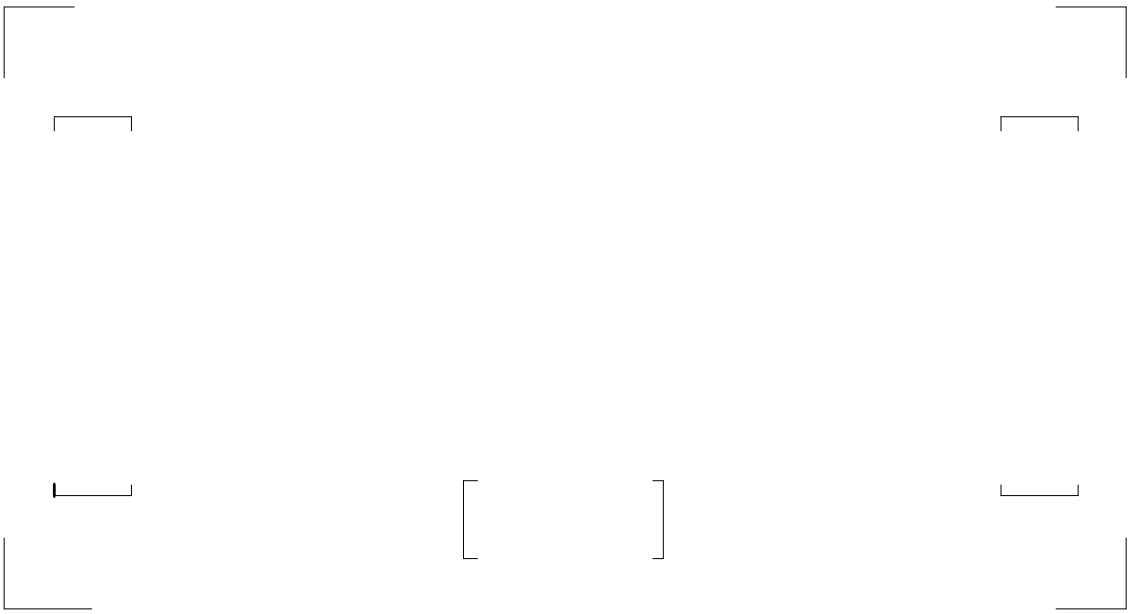
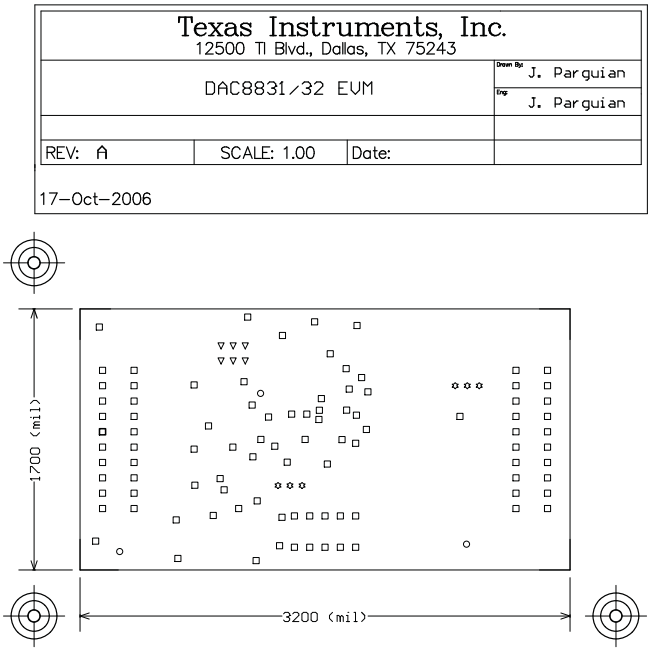


**Figure 5. Bottom Silkscreen**




Notes:

1. PWB to be manufactured RoHS compliant and marked as per IPC-1066.
2. PWB to be fabricated to meet or exceed IPC-6012, Class 3 standards workmanship shall conform to IPC-A-600 Class 3 - current revisions.
3. Board material and construction to be UL approved and marked on the finished board.
4. Laminate Material: Copper-clad FR-4 high Tg material; Tg >= 175 degrees C, Td >= 350 degrees C.
5. Copper Weight: 1 oz finished, all layers.
6. Finished Thickness: 0.062 +/- 0.010 inch.
7. Minimum plating thickness in through holes : 0.001 inch.
8. Board Finish : Immersion silver.
9. LPI soldermask both sides using appropriate layer artwork; color = green.
10. LPI silkscreen as required; color = white.
11. Vendor information to be incorporated on back side whenever possible.
12. Minimum copper conductor width is: 10 mils.
    Minimum conductor spacing is: 6 mils.
13. Number of finished layers: 2
14. Board dimensions: 3250 mils x 1700 mils

| | | | | |
|---|---|---|---|---|
| ○ | 3 | 37mil | 0.9398mm | PTH |
| ✲ | 6 | 32mil | 0.8128mm | PTH |
| ▽ | 6 | 27mil | 0.6858mm | PTH |
| □ | 96 | 15mil | 0.381mm | PTH |
| | 111 | Total | | |

**Figure 6. Drill Drawing**

## 2.2 EVM Performance Results

The EVM performance test is performed using a high density DAC bench test board, an Agilent 3458A digital multimeter and a PC running the LABVIEW software. The EVM board is tested for all codes of the device under test (DUT) and is allowed to settle for 1ms before the meter is read. This process is repeated for all codes to generate the measurements for INL and DNL results.

The results of the DAC8831/32 EVM characterization test are shown in Figure 7. Take note that the DAC8831/32 uses the OPA735 for the output buffer.

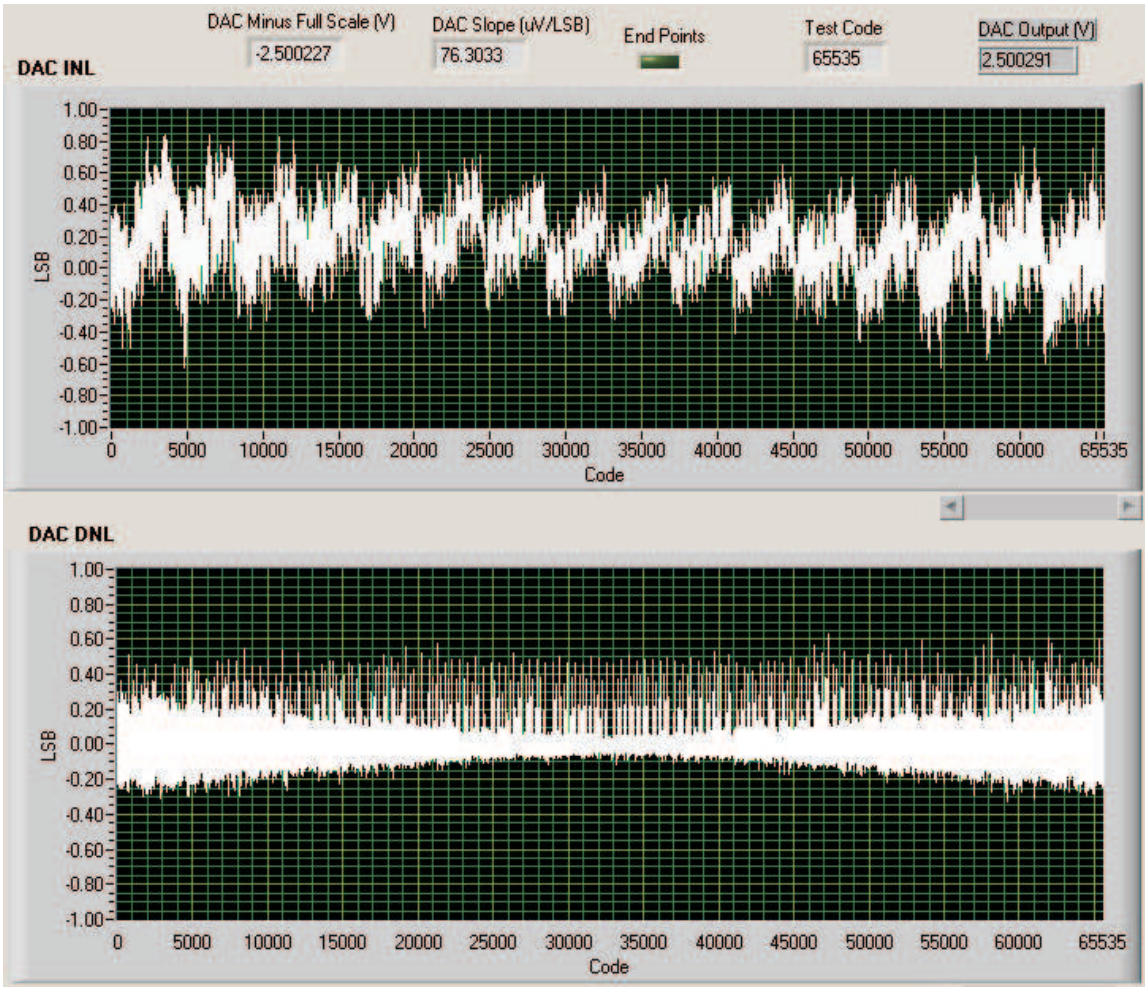



**Figure 7. INL and DNL Characterization Plot for the DAC8832**

## 2.3 Bill of Materials

**Table 2. Parts Lists**

| Item # | QTY | Designator | Manufacturer | Part Number | Description |
|---|---|---|---|---|---|
| 1 | 1 | C1 | TDK | C1608C0G1H101J | 100 pF, 0603, C0G, 50V, 5% Tol, Multilayer Ceramic Capacitor |
| 2 | 3 | C2 C3 C4 | TDK | C3216Y5V1C106Z | 10 µF, 1206, Y5V, 10V, 10% Tol, Multilayer Ceramic Capacitor |
| 3 | 4 | C5 C7 C10 C11 | TDK | C2012X7R1E104K | 0.1 µF, 0805, X7R, 50V, 10% Tol, Multilayer Ceramic Capacitor |
| 4 | 3 | C6 C8 C13 | TDK | C2012X7R1E104K | Not Installed |
| 5 | 1 | C9 | TDK | C2012X5R1A225M | 2.2 µF, 0805, Y5V, 10V, 10% Tol, Multilayer Ceramic Capacitor SMD |
| 6 | 1 | C15 | TDK | C2012X7R1E474M | 0.47 µF, 0805, Ceramic, Y5V, 10V, 10% Tol, Multilayer Ceramic Capacitor |
| 7 | 1 | J1 J2 (top side) | Samtec | TSM-110-01-T-DV-P | 10 Pin, Dual Row, SMT Header (20 Pos.) |

**Table 2. Parts Lists (continued)**

| Item # | QTY | Designator | Manufacturer | Part Number | Description |
|---|---|---|---|---|---|
| 8 | 1 | J1B J2B(bottom side) | Samtec | SSW-110-22-F-D-VS-K | 10 Pin, Dual Row, SMT Socket (20 Pos.) |
| 9 | 1 | J3 (top side) | Samtec | TSM-105-01-T-DV-P | 5 Pin, Dual Row, SMT Header (10 Pos.) |
| 10 | 2 | J3B (bottom side) | Samtec | SSW-105-22-F-D-VS-K | 5 Pin, Dual Row, SMT socket (10 Pos.) |
| 11 | 1 | R1 | Yageo America | 9C06031A1000JLHFT | 100 Ω, 0603, 5%, 0.1 W resistor |
| 12 | 1 | R2 W2 W4 | Yageo America | 9C06031A0R00JLHFT | 0 Ω, 0805, 5%, 0.1 W resistor |
| 13 | 1 | R3 R4 R7 | | | Not Installed |
| 14 | 2 | R5 | Yageo America | 9C06031A33R0JLHFT | 33 Ω, 0603, 5%, 0.1 W resistor |
| 15 | 2 | R6 | Yageo America | 9C06031A1002JLHFT | 10 kΩ, 0603, 5%, 0.1 W resistor |
| 16 | 1 | SW1 | E Switch | EG2209 | DPDT Slide Switch |
| 17 | 1 | TP2 | Keystone | 5001 | Red Test Point Loop |
| 18 | 5 | DGND AGND | Keystone | 5000 | Black Test Point Loop |
| 19 | 2 | U1 | Texas Instruments | OPA735AIDBVT | OPA735 |
| 20 | 1 | U2 | Texas Instruments | OPA735AIDBVT | Not Installed – Optional Component |
| 21 | 3 | U3 | Texas Instruments | DAC8831ICRGY | 16-Bit, Unbuffered Voltage Output, Reset to Zero-Scale DAC |
| | | | | DAC8832ICRGY | 16-Bit, Unbuffered Voltage Output, Reset to Mid-Scale DAC |
| 22 | 3 | U4 | Texas Instruments | OPA353NA | OPA353 |
| 23 | 1 | U5 | Texas Instruments | REF3025AIDBZT | REF3025 |
| 24 | 1 | W1 W3 | Samtec | TSW-103-07-L-S | 3 Pin, Single Row, TH Header |
| NOTE: P2, P4 & P6 parts are not shown in the schematic diagram. All the P designated parts are installed in the bottom side of the PC Board opposite the J designated counterpart. Example, J2 is installed on the topside while P2 is installed in the bottom side opposite of J2. The following parts; J1, J3, R1, R2 and R3 are not installed. | | | | | |

# 3 EVM Operation

This chapter covers in detail the operation of the EVM to provide guidance to the user in evaluating the onboard DAC and how to interface the EVM to a host processor.

Refer to the specific DAC data sheet, as listed in the *Related Documentation from Texas Instruments* section of this user's guide for more information about the DAC's serial interface and other related topics.

The EVM board is factory tested and configured to operate in the bipolar output mode.

## *3.1 Factory Default Setting*

The EVM board is set to its default configuration from factory as described in Table 3 to operate in bipolar ±2.5V output operation. The default jumper settings are shown in Figure 8.

**Table 3. DAC8831/32 EVM Factory Default Jumper Setting**

| DAC8831/32 EVM JUMPER DEFAULT CONFIGURATION | | |
|---|---|---|
| **Reference** | **Jumper Position** | **Function** |
| W1 | 1-2 | Controls DAC reference source (default is U5 at 2.5VDC) |
| W3 | 1-2 | Controls LDAC pin (default is DGND) |
| SW1 | RIGHT | Controls analog output voltage (default is ±Vref) |
| R2 | INSTALLED | Powers output buffer, U1 with ±5 V supplies. |

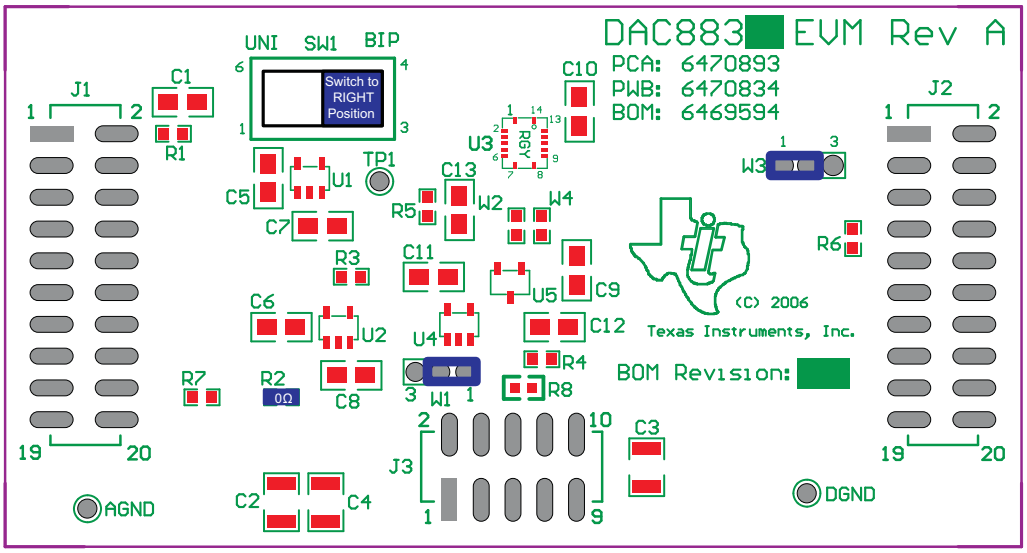



**Figure 8. DAC8831/32 EVM Default Configuration Setting**

## 3.2 Host Processor Interface

The host processor basically drives the DAC, so the DACs proper operation depends on the successful configuration between the host processor and the EVM board. In addition, a properly written code is also required to operate the DAC.

A custom cable can be made specific to any host interface platform that the EVM user chooses to use. The EVM board allows interface to the host processor through J2 header connector for the serial control signals and the serial data input. The output can be monitored through the J1 header connector.

To alleviate the tedious task of building customize cables, the DAC8831/32 EVM is designed based on the modular EVM form factor from Texas Instruments. This EVM form factor allows direct evaluation of the DAC's performance and operating characteristics in conjunction with the 5-6K (SLAU104), and the HPA-MCU (SLAU106) Interface Boards from Texas Instruments.

In addition, a third party board such as the HPA449 Demonstration Board from SoftBaugh, Inc. (www.softbaugh.com) can also be used. Field Programmable Gate Array (FPGA) users may also use the DAC8831/32 EVM in conjunction with a variety of Xilinx FPGAs by obtaining the Texas Instruments Analog Adapter Kit (part number ADS-TI-AD-DAU) from Avnet Electronics Marketing.

Using the interface cards mentioned above to evaluate the DAC8831/32 EVM allows easy configuration of a simple evaluation system.

This DAC EVM interfaces with any host processor capable of handling serial communication protocols or the popular TI DSP of up to 50MHz clock speed. For more information regarding the serial interface of the particular DAC installed, please refer to the specific DAC data sheet, as listed in the *Related Documentation from Texas Instruments* section of this user's guide.

## 3.3 Analog Interface

For maximum flexibility, the DAC8831/32 EVM is designed for easy interfacing to multiple analog sources. Table 4 provides the pinout of connector J1. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient 10-pin, dual-row header/socket combination at J1. This header/socket provides access to the analog output pins of the DAC through the onboard buffer amplifier. Consult Samtec at www.samtec.com, or call 1-800-SAMTEC-9 for a variety of mating connector options.

**Table 4. Pinout of J1**

| Pin Number | Signal | Description |
|---|---|---|
| J1-2 | Vout | Buffer voltage output – range depends on the position of SW1 (see section 3.3.1) |
| J1-4 | Unused | Pins are unused and should be left open for use with future amplifier and sensor output modules. |
| J1-6 | Unused | |
| J1-8 | Unused | |
| J1-10 | Unused | |
| J1-12 | Unused | |
| J1-14 | Unused | |
| J1-16 | Unused | |
| J1-18 | REF(–) | Unused |
| J1-20 | REF(+) | External reference source input (1.25 V to 5.5 V maximum) |
| J1-15 | Unused | |
| J1-1–J1-19 (odd) | AGND | Analog ground connections (except J1-15) |

### 3.3.1 EVM Output Voltage

Switch SW1 provides a means to allow unipolar or bipolar output operation of the DAC8831/32 EVM. When the slide switch is to the right (screen marked BIP), the output voltage on J1-2 is ±VREF. If the onboard reference is used, this means that the output voltage is –2.5 Vdc to +2.5 Vdc. When the switch is to the left (screen marked UNI), the output from the buffer is 0 V to +2.5 Vdc.

For a wider dynamic output range, the EVM can be configured to use an external reference by moving the shunt at W1 to cover pins 2-3. In this case, an external reference from 1.25V to VDD may be applied to J1-20. For best performance, the external reference must be supplied by a clean dc source. Take note that the DAC output voltage may be limited by the input/output operating rails of the chosen output amplifier.

## 3.4 Digital Interface Control

The DAC8831EVM is designed for easy interfacing to multiple control platforms. Table 5 provides the pinout of connector J2. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient 10-pin dual row header/socket combination at J2. This header/socket provides access to the digital control and serial data pins of the DAC8831EVM. Consult Samtec at www.samtec.com, or call 1-800-SAMTEC-9 for a variety of mating connector options.

The digital control signals can be applied directly to J2 (top or bottom side). The DAC8831/32 EVM can also be connected directly to a DSP or microcontroller interface board such as the 5-6K Interface Board, the HPA-MCU Interface Board or the HPA449 as mentioned earlier. See the DAC8831 or the DAC8832 product folder on the TI Web site (www.ti.com) for a current list of compatible interface and/or accessory boards.

**Table 5. Pinout of J2**

| Pin Number | Signal | Description |
|---|---|---|
| J2-1 | Unused | |
| J2-3 | SCLK | Serial Clock |
| J2-5 | Unused | |
| J2-7 | $\overline{CS}$ | Select to the DAC. Tied to the Frame Sync for DSP host systems – STE for SPI™ Host systems |
| J2-9 | Unused | |
| J2-11 | SDI | Serial Data Input |
| J2-13 | Unused | |
| J2-15 | Unused | |
| J2-17 | $\overline{LDAC}$ | Load DAC – Active low signal; enables DAC output updates – jumper configurable (see schematic). When LDAC is Low, the DAC latch is simultaneously updated with the content of the input register. Can be controlled by GPIO or tied low via W3. |
| J2-19 | Unused | |

## 3.5 Analog Output

The analog output is applied directly to J1 (top or bottom side) and can be further applied to optional amplifier and signal conditioning modules. The analog output range depends on the configuration of the EVM and the external reference applied at J1-20 or TP2. See section 3.1 of this user's guide and the DAC8831 data sheet (SLAS449) or the DAC8832 data sheet (SBAS380) to determine the maximum analog output range.

## 3.6 Load DAC ($\overline{LDAC}$)

Jumper W2 is provided to allow the selection of the signals applied to the DAC8831 or DAC8832 LDAC pin. The factory default condition for the EVM is to place a shunt jumper between pins 1-2 of W3. This ties the $\overline{LDAC}$ pin directly to ground for simultaneous updates of the DAC output buffer. When the shunt is moved to pins 2-3, an external $\overline{LDAC}$ signal may be applied to J2-17 to allow timed updates of the DAC output buffer.

## 3.7 Jumper and Switch Setting

Table 6 shows the function of each specific jumper setting of the EVM.

**Table 6. Jumper Setting Function**

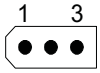
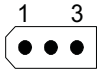
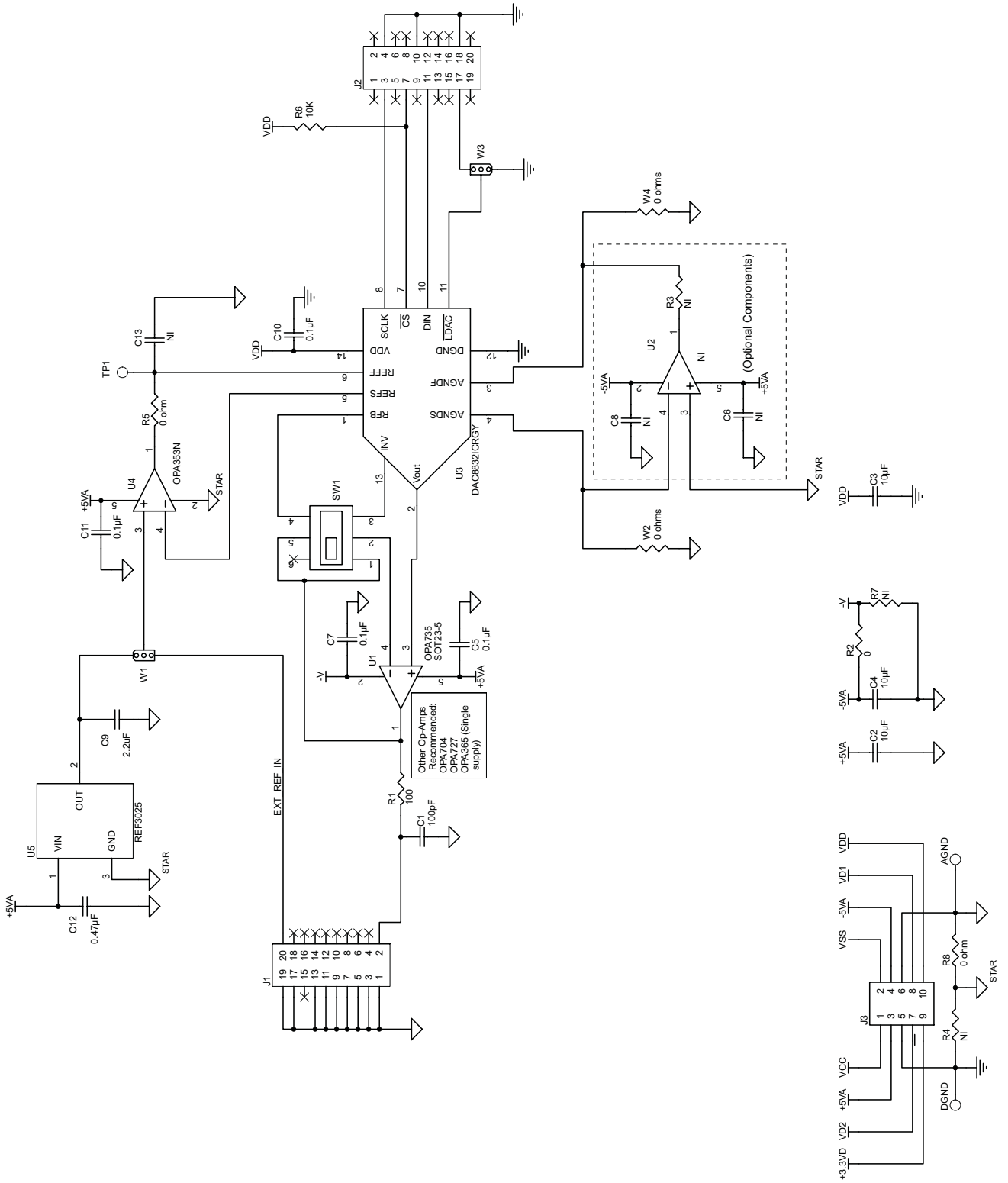
| Reference | Jumper Setting | Function |
|---|---|---|
| W1 |  | Routes the 2.5V reference from U5 through buffer U4 for DAC VREF pin. |
| |  | Disconnect the onboard (U5) and external (via J1-20) references and use desired source of reference applied directly into W1-2. |
| |  | Routes the external reference source from J1-20 through buffer U4 for DAC $V_{REF}$ pin. |
| W3 |  | $\overline{LDAC}$ pin is tied directly to ground. Puts the DAC into transparent mode. |
| |  | $\overline{LDAC}$ pin is not connected. |
| |  | $\overline{LDAC}$ pin is tied directly to J2-17. Allows the host controller to update the DAC output simultaneously. |

**Table 6. Jumper Setting Function (continued)**

| Reference | Jumper Setting | Function |
|---|---|---|
| SW1 |  | DAC is in unipolar mode of operation. |
| |  | DAC is in bipolar mode of operation. |
| **Legend:** |  | Indicates the corresponding pins that are shorted or closed. |

## 3.8 Schematics



## EVALUATION BOARD/KIT IMPORTANT NOTICE

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. Persons handling the product(s) must have electronics training and observe good engineering practice standards. As such, the goods being provided are not intended to be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety and environmental measures typically found in end products that incorporate such semiconductor components or circuit boards. This evaluation board/kit does not fall within the scope of the European Union directives regarding electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE or UL, and therefore may not meet the technical requirements of these directives or other related directives.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

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## EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range specified in Table 1 (±5 VDC), and an output voltage range of ±5 VDC.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 30°C. The EVM is designed to operate properly with certain components above 30°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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